

WHAT IS CLAIMED IS:

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1. A packet data processing apparatus for processing a packet received from a network by a processor, comprising:

10 a packet data access part, which has a plurality of registers arranged in series, shifting the received packet through the plurality of registers toward an outlet in synchronization with a clock,

15 wherein the processor processes the received packet while the received packet is being shifting through the plurality of registers.

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2. The packet data processing apparatus as claimed in claim 1, further comprising:

25 an intermediate data maintaining part, which has a plurality of registers arranged in series, sequentially shifting intermediate data showing a process result of the received packet through the plurality of registers toward the outlet in synchronization with the clock.

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3. The packet data processing apparatus as claimed in claim 1, further comprising a search
35 table, wherein said processor searches the search table by using data of the received packet, and retrieves information corresponding to the data of

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4. The packet data processing apparatus as claimed in claim 1, wherein said processor processes the received packet being shifted by said packet data access part in accordance with a set of instructions.

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5. The packet data processing apparatus as claimed in claim 4, wherein the set of sequential instructions is for executing a checksum calculation for the received packet.

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25 6. The packet data processing apparatus as claimed in claim 4, wherein the set of sequential instructions is for executing a Time-To-Live calculation for the received packet.

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30 7. The packet data processing apparatus
as claimed in claim 1, further comprising a search
table, wherein said processor searches said search
table for transmission interface information by using
35 a destination address stored in the received packet,
and retrieves the transmission interface information
corresponding to the destination address, in

accordance with a set of instructions for forwarding the received packet to the destination address while the received packet is shifted by said packet data access part.

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8. A packet relay apparatus for forwarding a packet received from a network, comprising:

a plurality of processors being connected in series, each processor comprising:

a packet data access part, which has a plurality of registers arranged in series, shifting the received packet through the plurality of registers toward an outlet in synchronization with a clock,

wherein the processor processes the received packet while the received packet is being shifting through the plurality of registers.

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9. The packet relay apparatus as claimed in claim 8, wherein each processor independently processes the received packet being shifted by said packet data access part in accordance with a different instruction order.

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10. The packet relay apparatus as claimed in claim 8, further comprising:

a shared data access part, which has at

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a send-position changing part changing a send-position of said plurality of registers of the packet data access part where the send-position defines an outlet point at which said packet data access point sends the packet to an exterior thereof.